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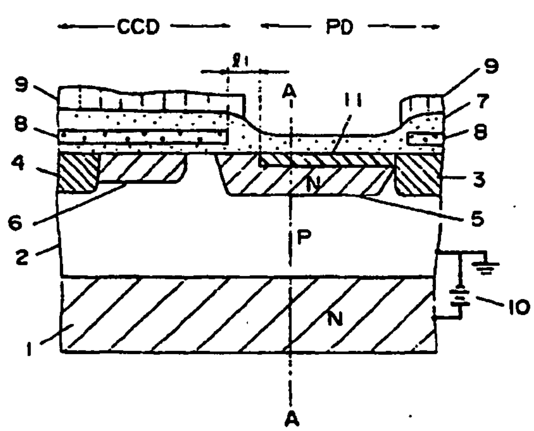
(54) **Solid state image sensor.**

(57) In this invention, in the principal surface portion of an impurity region of first conductive type composing à PN junction photo diode, an impurity region of reverse conductive type is formed in the almost entire region except for a part of side area of an electric charge reading part. When the impurity region of reverse conductive type is formed in the principal surface portion of the impurity region of one conductive type, the interface trap level generated in the interface of the semiconductor substrate and silicon dioxide film on its surface can be reduced, so that the generation of dark current may by significantly decreased.

FIG. 1



EP 0 360 595 A2

Description

SOLID STATE IMAGE SENSOR

This invention relates to a solid state image sensor used in a video camera and the like.

A change coupled delvce (CCD) solid state image sensor, in particular, an interline transfer type CCD solid state image sensor possesses an excellent resolution and a high photo-sensitivity, and hence it has come to be used widely in video camera and other.

FIG. 6 is a sectional view of a unit cell of a conventional interline transfer type CCD image sensor using a PN junction photo diode as photo detector.

In FIG. 6, one unit cell of a solid state image sensor is composed of a photo detector (PD) and a charge reading unit (CCD). A P-type well 2 is formed on an N-type silicon substrate 1. Near the surface in the P-type well 2, P-type channel stop regions 3, 4 for isolating the adjacent unit cells are formed. These channel stop regions 3, 4 are connected to the grounding potential. Closely to one channel stop region 3 in the P-type well 2, an N-type region 5 diffusing on N-type impurity is formed, and a PN junction photo diode of the photo detector (PD) is formed by the P-type well 2 and N-type region 5. Closely to the other channel stop region 4 in the P-type well 2, and N-type region 6 diffusing an N-type impurity is formed. This N-type region 6 is used as CCD transfer channel for sequentially transferring the signal electric changes generated in the photo detector (PD). The entire surface of the P-well 2 is covered with a silicon dioxide film 7. A polycrystalline silicon electrode 8 is buried in this silicon dioxide film 7. This polycrystalline silicone electrode 8 serves as both a reading gate for reading out signal electric changes from the N-type region 5, to the N-type region 6, and a CCD transfer gate. On the surface of the silicon dioxide film 7, an aluminum film 9 is formed. The aluminum film 9 cuts off the incident light into other parts that the photo diode. In order to allow the excessive electric charge to overflow into the N-type silicon substrate 1, a reverse bias voltage of the P-type wafer 2 is applied to the N-type silicon substrate 1 from a bias source 10. (This technique itself was disclosed, for example, in ISSCC Digest Technical Papers, pp. 168-169, 1982.)

Meanwhile, FIG. 6 shows only the portion for one unit cell of the CCD solid state image sensor, but actually multiple photo detectors (PD) and charge reading parts (CCD) are arranged in one row in a direction orthogonal to the surface of the paper, and further-more in a two-dimensional solid state image sensor, such photo detector (PD) row and charge reading part (CCD) row and arranged in multiple rows in a direction along the surface of the paper.

In such constitution, when an external light enters the photo diode through the silicon dioxide film 7 from the portion not covered with aluminum film 9, an electric charge is generated in the vicinity of the N-type region 5 and the P-type well 2 which compose the photo diode. The electric charges are read out into the N-type region 6 of CCD by applying a reading potential to the polycrystalline silicon electrode 8, and then, by alternately applying high potential and low potential to the multiple polycrystalline silicon electrodes 8 arranged in a direction orthogonal to the surface of the paper, the electric charges accumulated in the N-type region 6 are sequentially transferred in a direction orthogonal to the surface of the paper.

Incidentally in the conventional CCD solid state image sensor shown in FIG. 6, some of output current is observed even if the incident light is cut off completely. This is a kind of noise called dark current. The dark current is known to increase exponentially along with the temperature rise. Further, the following fact has been discovered in the experiment by the present inventors. The image lag characteristic is known as one of the important characteristics of the CCD solid stage image sensor. The image lag characteristic is determined by the structure of the photo diode. Therefore, usually, the image lag is suppressed by using a so-called complete depletion type photo diode. It was, however, found that the dark current increases when the photo diode of complete depletion type is used in order to improve the image lag characteristic.

When the dark current increases, the ratio of the dark current (N) to signal current (S) increases, particularly at low illumination intensity, and the so-called S/N ratio deteriorates. Besides, if the amplitude of dark current varies in each photo diode, the fixed pattern noise increases when the illumination intensity is low or temperature is high.

Therefore, in order to improve the overall characteristics of the CCD solid state image sensor, it is extremely important to suppress the dark current itself and the fluctuations of the amplitude of dark current in multiple photo diodes.

It is hence a first object of this invention to present a solid state image sensor capable of suppressing the dark current.

It is a second object of the invention to present a solid state image sensor capable of suppressing the fluctuations of the dark current among plural photo diodes.

This invention, in sum, is characterized by formation of a reverse conductive type impurity region in a principal surface region of an impurity region of one conductive type composing the photo diode except for a part of CCD side.

When an impurity region of reverse condcutive type is formed in the principal surface portion of the impurity region of one conductive type, the interface trap level formed in the interface between the semi-conductor substrate and the silicon dioxide film on its surface may be reduced, and hence the generation of dark current may be significantly decreased.

Other objects of the invention will be more clearly understood and appreciated from the following detailed description of the embodiments taken in conjunction with the drawings.

FIG. 1 is a sectional view of a portion of one unit cell of a solid state image sensor in a first embodiment of the invention;

FIG. 2 (a) is a drawing showing a potential profile along line A-A in FIG. 1;

FIG. 2 (b) is a drawing showing a potential profile along line A-A in FIG. 6;

FIG. 3 (a) to (d) are sectional views sequentially showing the manufacturing method of a solid state image sensor according to a second embodiment of the invention;

FIG. 4 is a sectional view of a portion of one unit cell of the solid state image sensor in the second embodiment;

FIG. 5 is a sectional view of a portion of one unit cell of the solid state image sensor in a third embodiment of the invention; and

FIG. 6 is a sectional view of a portion of one unit cell of a conventional solid state image sensor.

FIG. 1 is a sectional view of a first embodiment of a solid state image sensor of the invention, and in FIG. 1, too, same as in FIG. 6, only one unit cell of the interline transfer type CCD solid state image sensor using the PN junction photo diode as photo detector is shown.

In FIG. 1, the parts substantially having the same functions as the conventional CCD solid state image sensor shown in FIG. 6 are identified with the same reference numerals, and the detailed explanation is emitted.

As evident from the comparison between FIG. 1 and FIG. 6, in FIG. 1, a P-type region 11 injecting or diffusing a P-type impurity is formed in the surface portion of the N-type region 5 forming the photo diode. One edge of the P-type region 11 is located at a position remote from one edge of a polycrystalline silicon electrode 8 by distance ℓ_3, while the other edge of the P-type region 11 is connected to the P-type channel stop region 3. Therefore, the P-type region 11 is connected to the grounding potential through the channel stop region 3. In this embodiment, meanwhile, the junction depth of the P-type region 11 is 0.5 µm and the surface impurity concentration is $2 \times 10^{18}/cm^3$.

5 Mic

≈500Å

Several causes are considered for generation of dark current, but as a result of the experiment by the present inventors, it has been discovered that the depleted region formed in the interface between the silicon substrate and the silicon dioxide film on its surface is a principal source of dark current. Also seeing from the fact, as stated above, that the dark current increases when the photo diode of complete depletion type is used in order to improve the image lag characteristic, it is known that the depleted region in the interface of the substrate and silicon dioxide film is a dominant factor for generation of dark current.

That is, in the conventional CCD solid state image sensor shown in FIG. 6, depleted region is formed in the interface of the P-type well 2 ad N-type region 5, and also in the interface of the N-type region 5 and silicon dioxide film 7. Of them, the depleted region formed in the interface of the N-type region 5 and silicon dioxide film 7, in other words, interface trap level existing in the interface makes easier to generate electrons. The current generated by these electrons becomes a main component of the dark current. Still more, as a result of damage or electrostatic breakdown in the plasma processing or ion processing steps in the semiconductor processing steps, the density of interface trap level increases. Further the density of interface trap level increases exponentially along with the temperature rise, so that the dark current increases as a matter of course.

Accordingly, in the first embodiment of the invention shown in FIG. 1, the P-type region 11 is formed in the portion where the interface tape level is generated, that is, in the interface of the N-type region 5 and the silicon dioxide film 7, and this P-type region 11 is connected to the grounding potential through the P-type channel stop region 3.

FIG. 2 (a) shows a potential profile along line A-A in FIG. 1. Immediately beneath the silicon dioxide film 7, an interface trap level 12 is generated as schematically indicated by X in FIG. 2 (a). On the other hand, FIG 2 (b) shows a potential profile along line A-A in FIG. 6. In the conventional structure shown in FIG. 6, since the N-type region 5 was formed immediately beneath the silicon dioxide film 7, the potential profile continues flatly from the N-type region 5 to the interface with the silicon dioxide film 7 as shown by reference numeral 13 in FIG. 2 (b). Therefore, the electrons generated from the interface trap level flow into the N-type region 5, which causes the dark current. By contrast, in the structure of the first embodiment of the invention shown in FIG. 1, the P-type region 11 is buried in the surface portion of the N-type region 5, and this P-type region 11 is connected to the grounding potential. Accordingy, the potential profile is fixed at 0V in the P-type region 11 as shown in FIG. 2 (a). As a result, the electrons generated at the interface trap level disappears by re-combining with holes through the P-type region 11. Therefore, the electrons generated at the interface trap level do not flow into the N-type region 5, and hence the dark current is suppressed notably.

To suppress the dark current, meanwhile, it is desired to bury the P-type region 11 in the entire surface of the N-type region 5. Thus, the affects of the interface trap level in the region indicated by ℓ_1 in FIG. 1 may be also suppressed. However, when ℓ_1 is set at about 0.5 µm, that is, about the depth of function of the P-type region 11, the P-type impurity is diffused nearly to the lower part of the polycrystalline silicon electrode 8, which may affect the potential profile in the reading action of the signal electric charge. Hence, the image lag due to imperfect pickup of the signal electric change may be likely to occur. Therefore, the value of ℓ_1 must be determined considering the shape of photo diode and impurity profile of N-type region 5 etc. In the embodiment shown in FIG. 1, setting ℓ_1 at 0.8 µm, the P-type region 11 was formed in about 80 percent of the surface area of the N-type region 5. At this time, the dark current was decreased to about 25% of the conventional level.

In the embodiment in FIG. 1, the impurity

concentration of the P-type region 11 is 2 x $10^{18}/cm^3$. According to the experiment by the present inventors, when the impurity concentration of P-type region was in the order of 10^{17}, the stability was poor, and in the order of 10^{18} or more, depletion of the interface in the ordinary operation could be prevented, and the dark current could be stably suppressed.

Meanwhile, in the first embodiment of the invention shown in FIG. 1, the structure of the reading gate parts of CCD, that is, the N-type region 6, polycrystalline silicon electrode 8 and others may be same as in the conventional structure. Therefore, the characteristics relating to the functions of reading out signals are not changed at all. Therefore, it is not required to modify the external circuits connected to the CCD solid state image sensor.

In the embodiment in FIGS. 1, 2, it is intended to suppress the dark current itself, but actually the amplitude of dark current components is often different among multiple unit cells, and such fluctuation of the amplitude of dark current may lead to increasing noise, narrowing of dynamic range, and rough image of the entire picture as if seen through a ground glass at low illumination or high temperature.

Besides, as stated in relation to the embodiment in FIG. 1, when the distance ℓ_1 between the polycrystalline silicon electrode 8 and P-type region 11 is narrowed, the dark current decreases, but the potential profile in the overlap area of the polycrystalline silicone electrode 8 and N-type region 5 becomes higher due to the effect of the P-type region 11. Accordingly, the image lag is likely to occur due to imperfect pickup of the signal electric charge in the reading action.

In order to suppress such fluctuation of amplitude of dark current and improve the image lag characteristic, it is extremely important to control the position of the P-type region 11 accurately with respect to the polycrystalline silicon electrode 8.

FIG. 3 (a) to (d) relate to a second embodiment of the invention, sequentially showing sectional views of manufacturing steps of a solid state image sensor capable of controlling the position of the P-type region 11 accurately with respect to the polycrystalline silicon electrode 8, and FIG. 4 is a sectional view showing its completion state. Both FIG. 3 and FIG. 4, same as FIG. 1, show only the unit cell portion of the interline transfer type CCD solid state image sensor using PN junction photo diode as photo detector, and the same parts as in FIG. 1 substantially are identified with same reference numerals.

Hereinafter the manfuacturing method is explained while referring to FIG. 3 (a) to (d).

First of all, as shown in FIG. 3 (a), a polycrystalline silicon electrode 8 is formed on a silicon dioxide film 7. Thereafter, the polycrystalline silicon electrode 8 is oxidized, and the silicon dioxide film 7 of about 2500 Å in thickness is formed on the surface and side face of the polycrystalline silicon electrode 8 [FIG. 3 (b)]. Next, as shown in FIG. 3 (c), boron ions (B^+) are injected from the surface of the silicon dioxide film 7 toward the substrate surface. In FIG. 3 (c), boron ions are injected through the silicon dioxide film 7, and at this time the silicon dioxide film at the side face of the polycrystalline silicon electrode 8 is thick, and therefore the polycrystalline silicon electrode 8 and the silicon dioxide film 7 at its side face work as masks when injecting ions. Accordingly, boron irons are injected into the region remote from the edge of the polycrystalline silicon electrode 8. The gap between the edge of the polycrystalline silicon electrode 8 and the boron injection region is determined by the film thickness of the silicon dioxide film 7 at the side face of the polycrystalline silicon electrode 8 grown in FIG. 3 (b). Therefore, by the heat treatment for about 1 hour at 900°C, the impurities of boron ions are diffused toward the polycrystalline silicon electrode 8, thereby forming a P-type region 11 in a shape partly overlapping with the polycrystalline silicon electrode 8 [FIG. 3 (d)].

Thereafter, by forming an aluminum film 9 for cutting off light on the surface of the silicon dioxide film 7, the unit cell portion as shown in FIG. 4 is completed.

In this manufacturing process, especially in the thermal diffusion step shown in FIG. 3 (d), when diffusing the boron ion impurities toward the polycrystalline silicon electrode 8, it is important to optimize the process conditions in order to suppressing the dark current and the image lag in reading out signal electric charges as far as possible. When such process conditions are optimized, the dark current may be sufficiently suppressed and the image lag characteristic may be satisfactorily maintained without having to keep a distance of ℓ_1 between the P-type region 11 and the polycrystalline silicon electrode 8 as in the first embodiment of the invention shown in FIG. 1. According to the expriment by the present inventors, even if the gap ℓ_2 in FIG. 4 (the overlapping width of polycrystalline silicon electrode 8 and N-type region 5) is set at 1.0 µm, longer than the junction depth 0.5 µm of the P-type region 11 and the P-type region 11 is diffused up to beneath the polycrystalline silicon electrode 8, the boron concentration profile beneath the polycrystalline silicon electrode 8 can be accurately controlled by optimizing the film thickness of the silicon dioxide film 7 at the side face of thepolycrystalline silicon electrode 8 in FIG. 3 (c) and the thermal diffusion conditions in FIG. 3 (d), and as a result the dark current characteristic and image lag characteristic can be improved at the same time.

Thus, the feature of the second embodiment of the invention disclosed in FIGS. 3, 4 is that the position or the area of the P-type region 11 is accurately controlled by self-alignment on the basic of the end portion of the polycrystalline silicon electrode 8. That is, in FIG. 3 (b), the film thickness of the silicon dioxide film 7 at the side face of the polycrystalline silicon electrode 8 can be accurately controlled. Besides, in FIG. 3 (c), since boron ions are injected by using the polycrystalline silicon electrode 8 and silicon dioxide film 7 as masks, the shape of the P-type region 11 can be accurately controlled. Moreover, when the heat treatment condition in FIG. 3 (d) is optimized, the boron concentration profile beneath the polycrystalline

silicon electrode 8 may be also controlled accurately.

Thus, according to the second embodiment shown in FIGS. 3, 4, since the shape of the P-type region 11 and impurity concentration beneath the polycrystalline silicon electrode 8 can be accurately controlled, fluctuations of amplitude of dark current among multiple unit cells may be suppressed. As a result, noise, dynamic range and image lag characteristics are greatly improved.

Incidentally, in the first and second embodiments shown in FIG. 1, FIG. 4, the aluminum film 9 for cutting off light is formed within the top area of the polycrystalline silicon electrode 8 or in a size slightly projecting from the end portion of the polycrystalline silicon electrode 8. Accordingly, the light obliquely entering the photo diode (PD) from upper right to the lower left corner of the drawing may pass near the end portion of the polycrystalline silicon electrode 8 to directly enter the CCD part. When the CCD directly receives an oblique incident light in this way, the signal electric charges due to the oblique incident light may be added to the original transfer electric charges during CCD reading period, and it may become a kind of false signal to make the image unclear, which is known as smear phenomenon.

FIG. 5 shows a third embodiment capable of solving such problem. FIG. 5 also shows, same as the first and second embodiments, only the unit cell portion of the interline transfer type CCD solid state image sensor using PN junction photo diode as the photo detector. In FIG. 5, the part substantially same in function as those in FIGS. 1, 3 are identified with same reference numerals, and the detailed explanation is omitted. On the surface of a silicon dioxide film 7, an aluminum film 14 for cutting off light is formed in the portion excluding the region of the photo diode (PD). As evident from FIG. 5, the end portion of the aluminum film 14 is formed so as to over the surface of the silicon dioxide film 7 at both sides of the polycrystalline silicon electrode 8. In this way, as shown in FIG. 5, the aluminum film 14 is extended to the photo diode (PD) by the total dimension of the film thickness ℓ_3 of silicon dioxide film 7 and the film thickness ℓ_4 of aluminum film 14. As a result, the oblique light entering the CCD part may be securely blocked at the end portion of the aluminum film 14, so that generation of smear may be notably suppressed.

In the foregoing embodiments, meanwhile, P-type well 2 is used as the substrate. By using the epitaxilaly grown P-type well 2 as the substrate, blooming and smear phenomena can be suppressed, and also it is effective to bring the spectral response closer to the response of the human eye.

Besides, in the foregoing embodiments, the excess electric charge is designed to overflow into the N-type silicon substrate 1, but a similar effect is obtained in a method of sweeping out the excess electric charge into the drain formed in the substrate surface portion.

Furthermore, in all of the embodiments herein, the N-type silicon substrate 1 is used, but it may be also possible, needless to say, to use the P-type silicon substrate.

Further, similar effects are also obtained when this invention is applied to the solid state image sensor of other types than the CCD type.

Claims

1. A solid state image sensor comprising:
a semiconductor substrate of first conductive type, and
plural unit cells formed in the surface portion of said semiconductor substrate, wherein
each one of said unit cells is composed of a photo detector and an electric charge reading part for reading out signal electric charge from said photo detector,
said photo detector is composed of said semiconductor substrate, and an impurity region of second conductive type formed in the principal surface portion of said semiconductor substrate, and
an impurity region of first conductive type is formed in the almost entire principal surface portion of said impurity region of second conductive type except for a part of the side area of said electric charge reading part.

2. A solid state image sensor according to claim 1, wherein said impurity region of first conductive type is connected to the grounding potential.

3. A solid state image sensor according to claim 1, wherein the impurity concentration of said impurity region of first conductive type is 1 x $10^{18}/cm^3$ or more.

4. A solid state image sensor according to claim 1, wherein a gap in a length of more than the junction depth of said impurity region of first conductive type is provided between one edge of said impurity region of first conductive type and one edge of the reading gate for composing said electric charge reading part.

5. A solid state image sensor according to claim 1, wherein a well of first conductive type formed on the surface of a semiconductor substrate of second conductive type is used as said semiconductor substrate of first conductive type.

6. A solid state image sensor comprising:
a semicondcutor substrate of first conductive type, and
plural unit cells formed in the surface portion of said semiconductor substrate, wherein
each one of said unit cells is composed of a photo detector and an electric charge reading part for reading out signal electric charge from said photo detector, and
said electric charge reading part is composed of a first insulation film formed on the principal surface of said semiconductor substrate, a reading gate formed on the surface of said first insulation film, a second insulation film formed on the surface and said face of said reading gate, and a light shielding film formed on the surface and side face of said second insulation film.

7. A solid state image sensor according to claim 6, wherein said photo detector is composed of said semiconductor substrate, and an impurity region of second conductive type formed in the principal surface portion of said semiconductor substrate, and an impurity region of first conductive type is formed in the almost entire principal surface portion of said impurity region of second conductive type except for a part of the side area of said electric charge reading part.

8. A solid state image sensor according to claim 6, wherein a well of first conductive type formed on the surface of a semiconductor substrate of second conductive type is used as said semiconductor substrate of first conductive type.

9. A solid state image sensor according to claim 7, wherein said impurity region of first conductive type is connected to the grounding potential.

10. A solid state image sensor according to claim 7, wherein the impurity concentration of said impurity region of first conductive type is 1 X $10^{18}/cm^3$ or more.

11. A manufacturing method of solid state image sensor comprising:
a step of forming an impurity region of second conductive type to compose a photo detector in the surface portion of a semiconductor substrate of first conductive type,
a step of forming a first insulation film of the surface of said semiconductor substrate and said impurity region of second conductive type,
a step of forming a reading gate for reading out electric charge on the surface of said first insulation film so as to partly overlapped with said impurity region of second conductive type,
a step of forming a second insulation film on the surface and side face of said reading gate.
a step of forming an impurity region of first conductive type in the surface portion of said impurity region of second conductive type, using said reading gate and said second insulation film formed on the side of said reading gate as the mask, and
a step of diffusing the impurity of said impurity region of first conductive type toward said reading gate side.

12. A manufacturing method of solid state image sensor according to claim 11, wherein said impurity region of first conductive type is connected to the grounding potential.

13. A manufacturing method of solid state image sensor according to claim 11, wherein the impurity concentration of said impurity region of first conductive type is 1 x $10^{18}/cm^3$ or more.

14. A manufacturing method of solid state image sensor according to claim 11, wherein a well of first conductive type formed on the surface of a semiconductor substrate of second conductive type is used as said semiconductive substrate of first conductive type.

FIG. 1

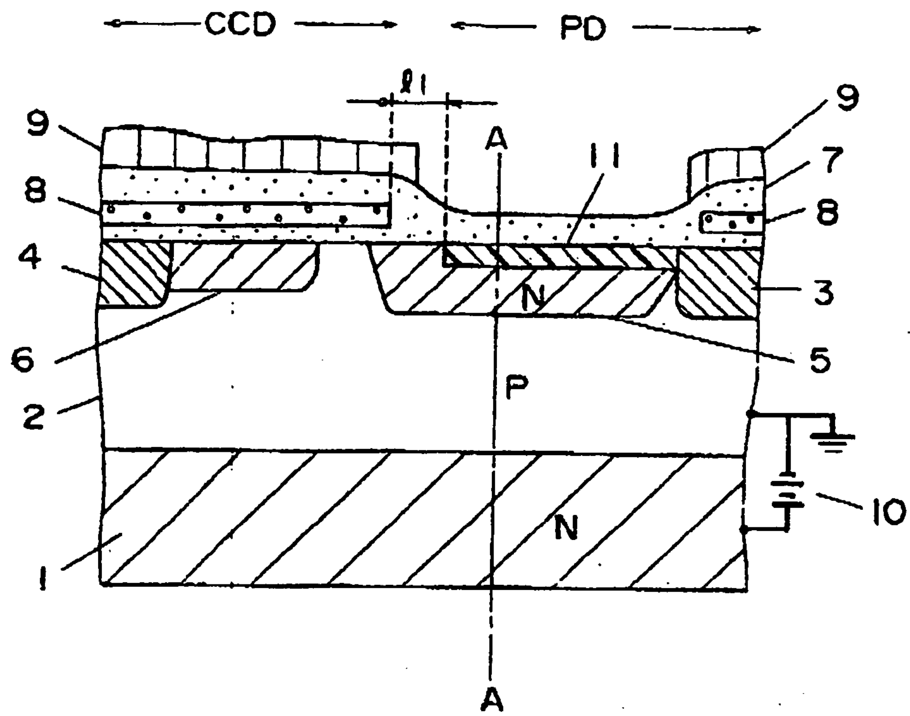


FIG. 2(a)

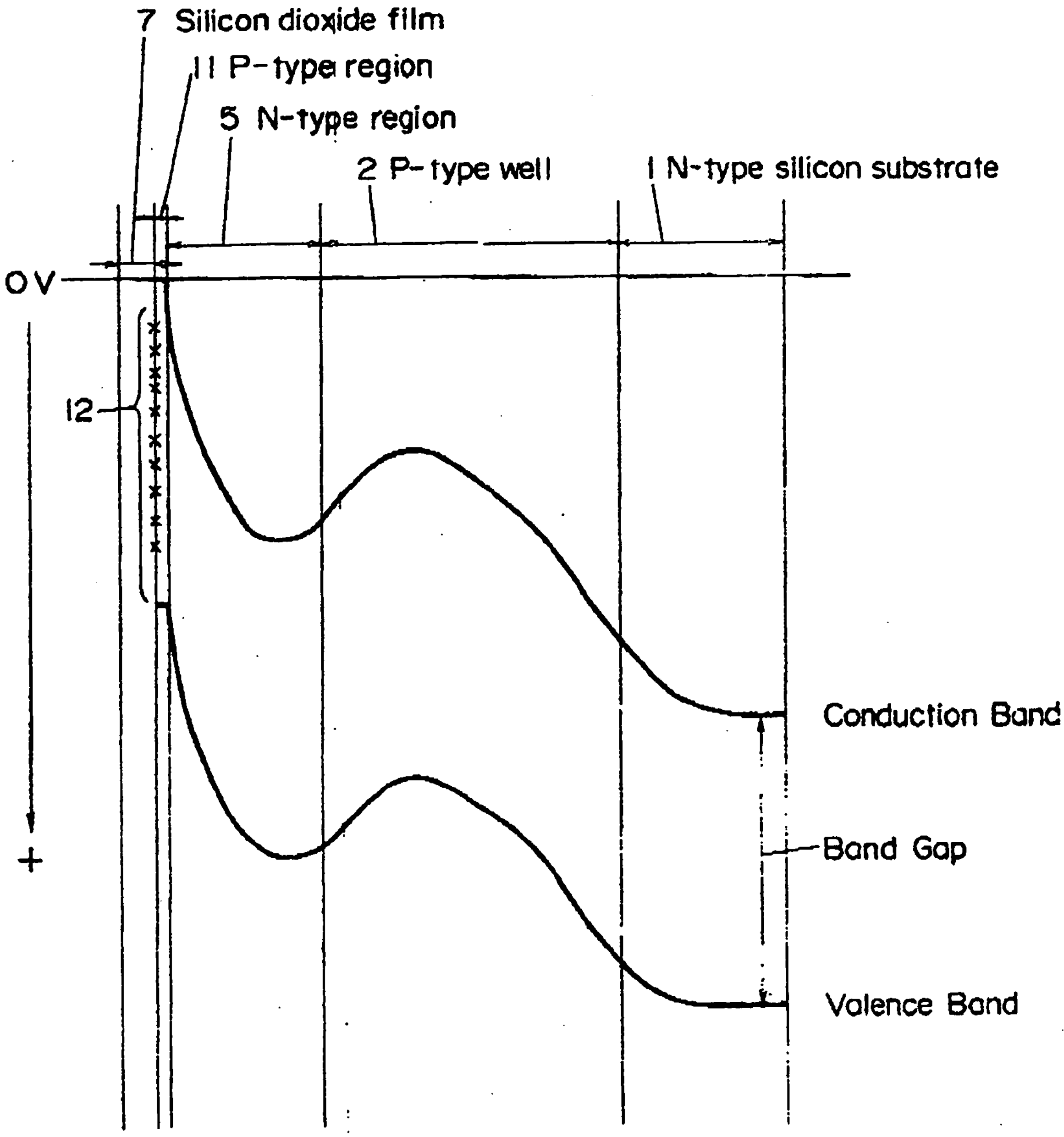

7 Silicon dioxide film
11 P-type region
5 N-type region
2 P-type well
1 N-type silicon substrate
OV
12
+
Conduction Band
Band Gap
Valence Band

FIG. 2(b)

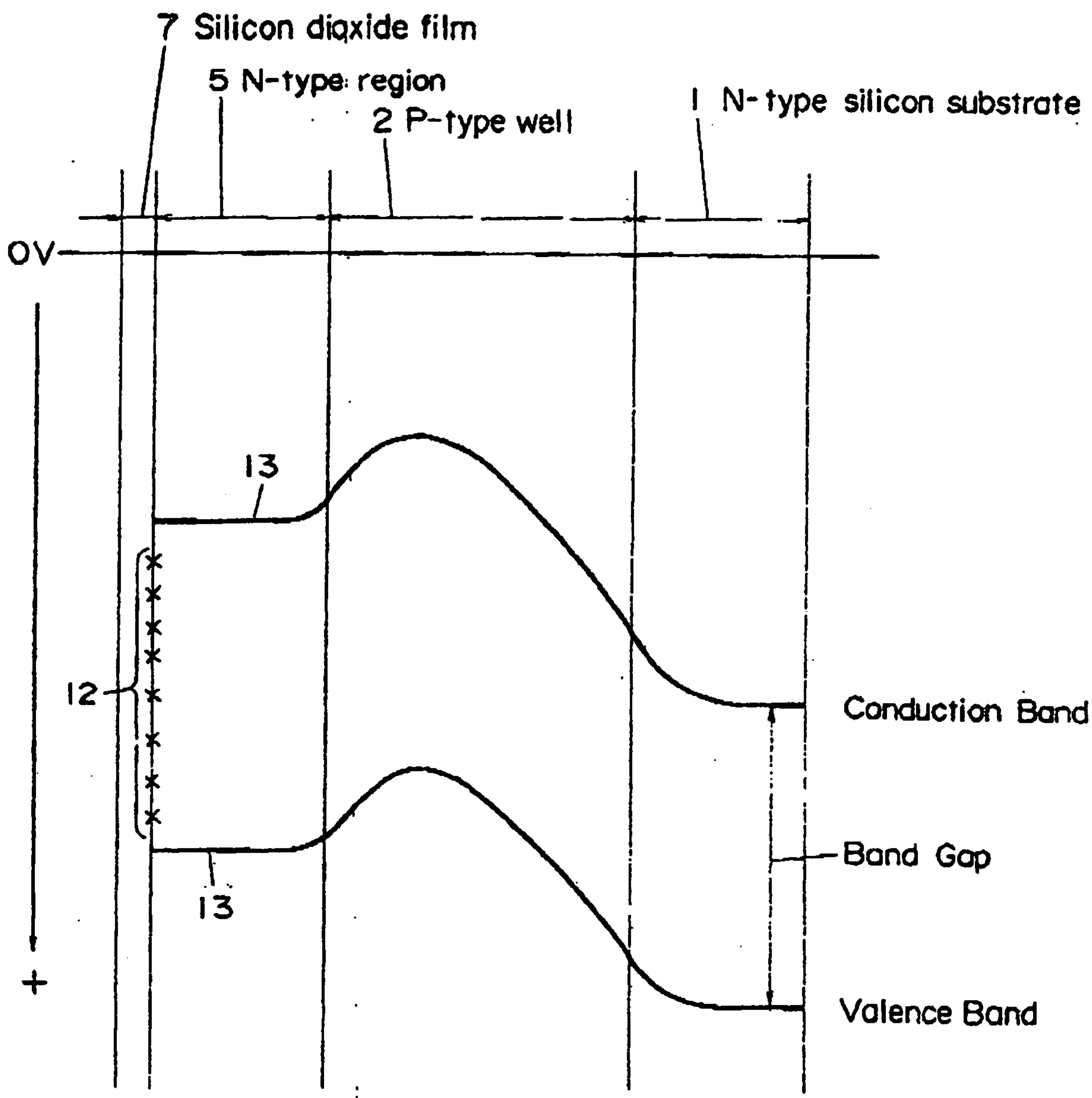

7 Silicon dioxide film
5 N-type region
2 P-type well
1 N-type silicon substrate
OV
13
12
13
+
Conduction Band
Band Gap
Valence Band

FIG. 3

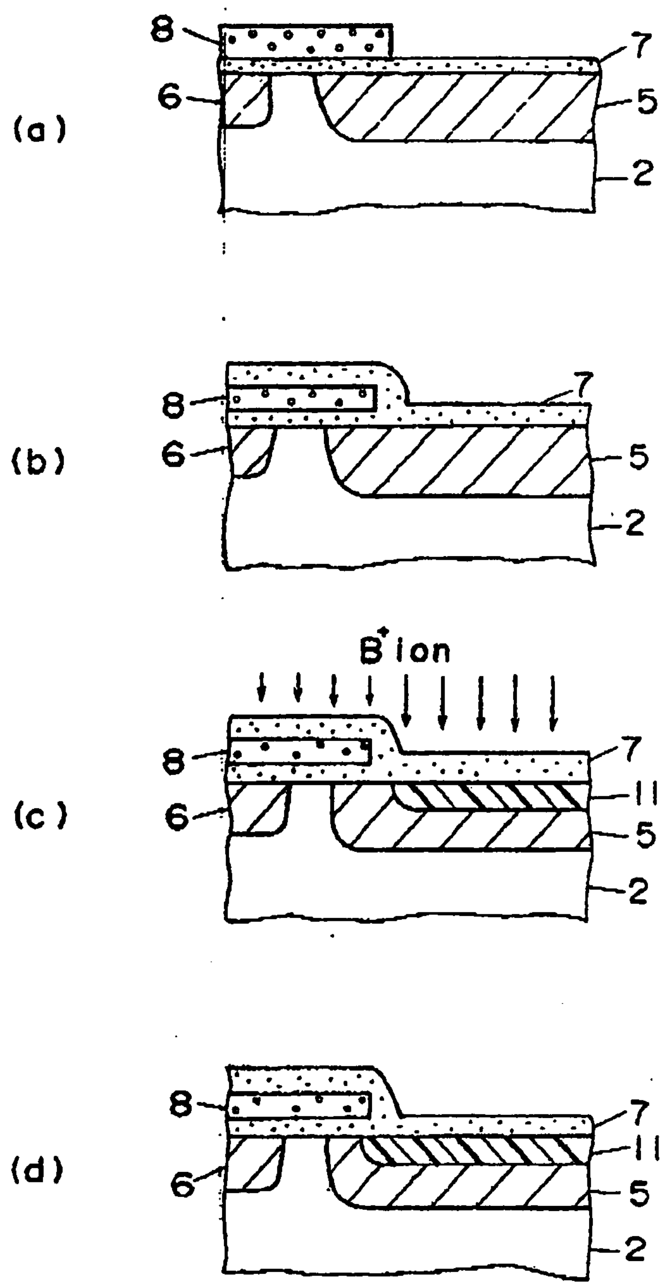


FIG. 4

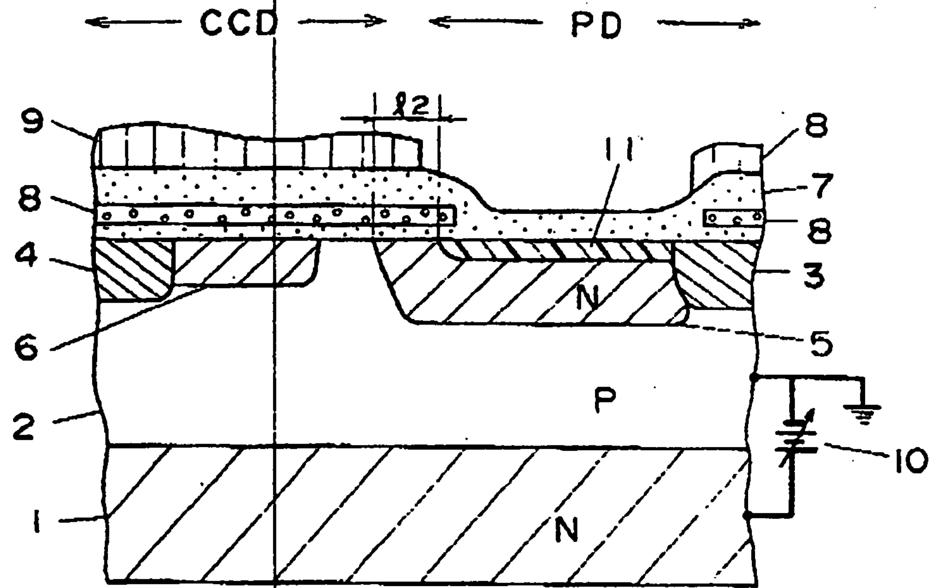

CCD
PD
ℓ2
9
8
11
8
7
8
8
4
3
N
6
5
P
2
10
1
N

FIG.5

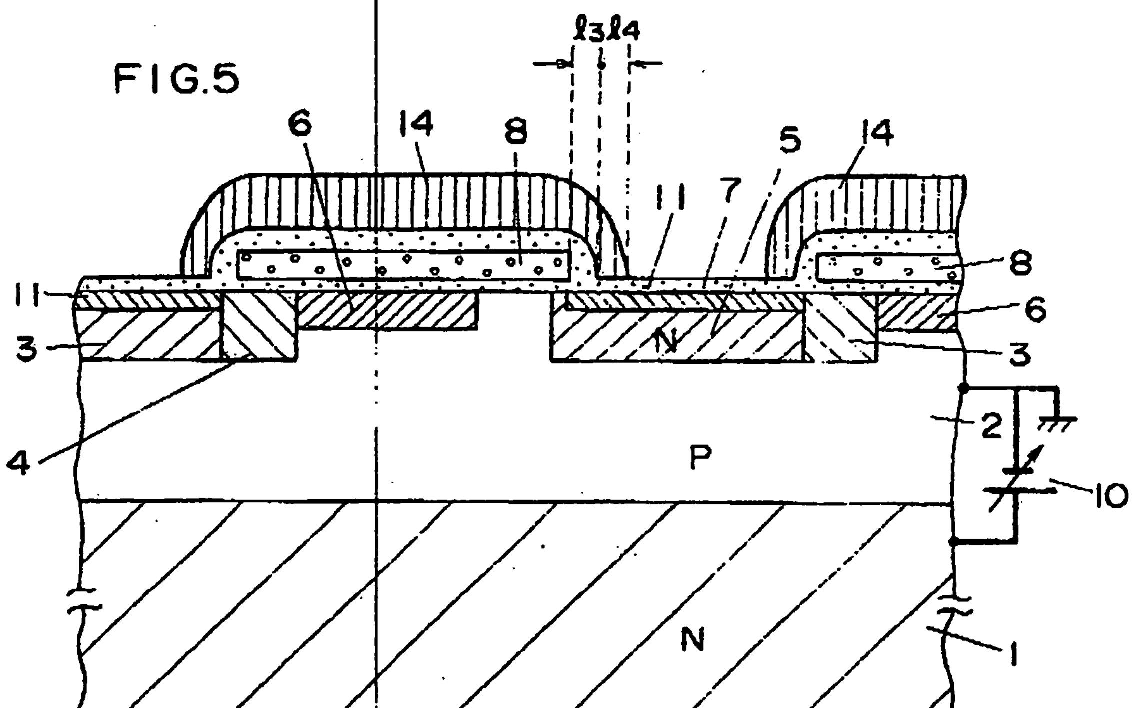
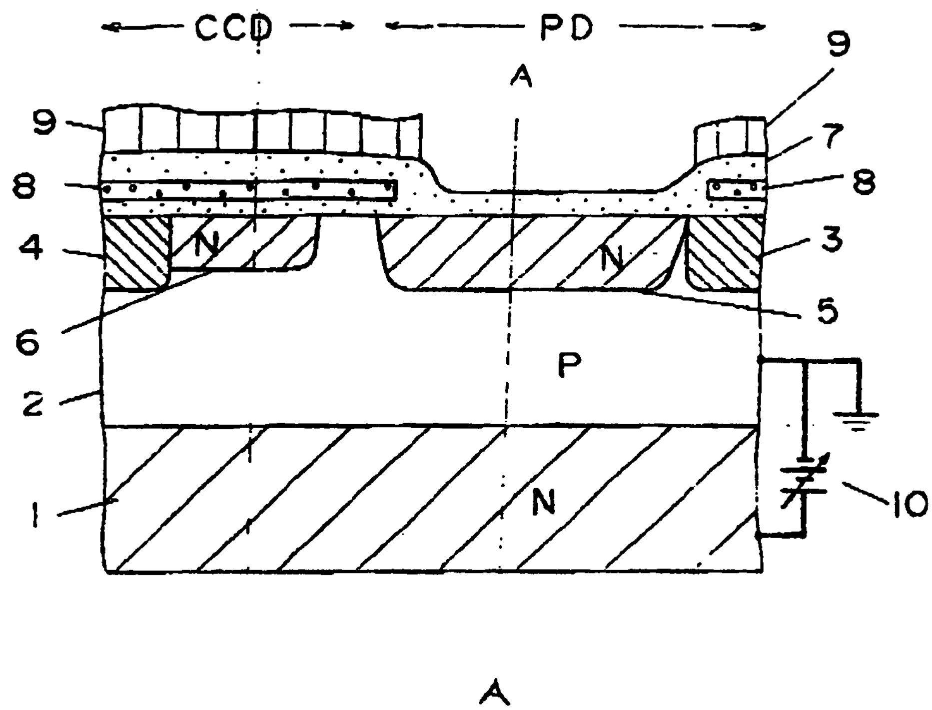

ℓ3ℓ4
6
14
8
5
14
11
7
8
11
6
3
N
3
4
2
P
10
N
1

FIG. 6



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EUROPEAN SEARCH REPORT

Application number
EP 89 30 9584

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int Cl 4)
X	IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, San Francisco, 22th-24th February 1984, vol. 27, Conf. 31, pages 32,33, IEEE; New York, US Y. MATSUNAGA et al.: "An inter-line transfer CCD imager" * Figur 1 *	1,4,5	H 01 L 27/148
Y		2,3,14	
	--		
X	INTERNATIONAL ELECTRON DEVICES MEETING; San franscisco, CA, 9th-12th December 1984, pages 28-31, IEDM B.C. BURKEY et al.: "The pinned photodiode for an interline-transfer CCD image sensor" * Figures 1,2; page 29, column 1, lower half *	11	
Y		12-14	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
	--		
X	WO-A-88 00 759 (KODAK) * Whole document *	6-9	H 01 L 27/00
Y		10	
	--		
Y	EP-A-0 224 993 (SHARP) * Figure 2; column 7, lines 48-50 *	2,12	
	--		
Y	EP-A-0 048 480 (NIPPON ELECTRIC) Figure 12; page 22, lines 14-20 *	3,10 13	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	01-02-1990	SINEMUS

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons
& : member of the same patent family, corresponding document

European Patent Office

	CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

X	LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,

namely:

1. Claims 1-5,11-14: Diffusion surface layer and process to produce it.
2. Claims 6-10: Light shield film formed on reading part.

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

namely claims:

☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims,

namely claims: